REMARKS

I. Pending Claims

Claims 1-3 and 5-10 were pending in the application after entry of the Preliminary Amendment filed October 23, 2001. Claims 2, 3 and 5-10 have been amended. Claims 1 and 9 have been cancelled and Claims 21-30 have been added in this amendment. Based upon the remarks below, allowance of the claims is respectfully requested.

II. Amendments To The Specification

The "Cross-Reference To Related Applications" section has been amended to indicate that the parent application of the current application is now issued as US Patent No. 6,365,924. In addition, to correct a typographical error, the Assignee of the current and parent applications has been identified as National Semiconductor Corporation.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "Version with markings to show changes made."

III. Amendments To The Claims

Claims 2, 3, 5-8 and 10 have been amended for formal matters and to correct typographical errors. Specifically, Claims 2, 3, 5-7 and 10 have been amended to recite "The ESD protection structure" as independent Claim 8, from which Claims 2, 3, 5-7 and 10 depend, recites "An ESD protection structure." This change is being made to correct a typographical error in the claims as originally filed.

Claims 2, 3, 5 and 10 have also been amended to depend from newly independent Claim 8, due to the cancellation of Claim 1, in order to have proper dependency.

Claim 8 has been amended to incorporate all of the limitation of independent Claim 1, which is now cancelled, from which Claim 8 previously depended.

IV. Claim Objections

Claims 1-3 and 5-10 are objected to due to the recitation, in Claim 1, of "said second conductor." Claims 2, 3 and 5-10 have been objected to due to the recitation, in each of the claims, of "the ESD structure" as opposed to "the ESD protection structure." Claims 8 and 9 have been objected to due to the recitation, in each of the claims, of "a terminal" as opposed to "said terminal."

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Claims 1 and 9 have been cancelled and the objections to those claims are now moot. Claims 2, 3 and 5-10 have been amended to recite "the ESD protection structure." Claim 8 is now independent and the recitation of "a terminal" is proper. Therefore, each of the claim objections is traversed.

V. Claim Rejections Under 35 U.S.C. § 112

Claims 8-10 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most clearly connected, to make and/or use the invention. The rejection with respect to Claim 8 and 10 is respectfully traversed. Claim 9 has been cancelled and the rejection with respect to Claim 9 is now moot.

Claim 8 and 10 are rejected because the recitations of "coupling of terminal A--first current source--first resistor--terminal K and the coupling of terminal A--second resistor--second current source--terminal K, and or the current sources each being back-to-back Zener diodes" are not enabled.

Specifically the Examiner states that the recitations are not enabled because the disclosure fails to describe: (1) how and by what means the current sources can be activated; (2) how a current source can be formed of a pair of back-to-back Zener diodes (see page 19, lines 13-26), given the fact that a diode itself can only serve as a voltage source; and (3) how the base of the bipolar transistor (130 or 150, Fig. 3) can be directly connected to both of the current source (770 or 772) and the resistor (756 or 758), given the fact that the base region is a lightly doped region, which itself always has residual resistance when connected to the outside.

With respect to (1) above, the specification clearly recites that "back-to-back Zener diode pair 852 and 854 act as a current source in branch 880 and back-to-back Zener diode pair 860 and 862 act as a current source in branch 890." (Page 18, ll. 13-15). Further, the specification recites that when "a positive voltage/current pulse is applied across terminals A and K, the voltage across diode 852 increases until diode 852 enters a reverse breakdown region," and diode 854 is forward biased to provide a voltage drop of nearly 0.65 volts across its two terminals." (Page 18, ll. 23-29). That is, during a positive ESD event from terminal A to K, the dv/dt across diode 852 will be greater than the dv/dt across diode 860 due to the presence of resistor 858 that also has its own voltage drop when a voltage is applied at

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terminal A. It is the rate of change in voltage across the Zener diodes that serve as the activation difference, in time, between the two current sources.

This time delay function is described in the specification at page 19, lines 3-8: "during the time period when diode 852 enters a reverse breakdown region, because of the presence of resistor 858 in branch 890, diode 860 does not enter a reverse breakdown region and, as such, no current flows through branch 890, preventing transistor 130 from being turned on." One of skill in the art would understand that the above means is that since branch 880, diodes 852 and 854, conduct first, ESD protection structure 100 conducts in the direction of the inherent transistor 150. That is because, only one of inherent transistor 130 or 150 can conduct at any given time. Therefore, the specification enables one of skill in the art to create a current source from diode pairs 852 and 854 and 860 and 862 that are triggered at different times due to the presence of resistors 856 or 858. This is inherent in the structures depicted in Figs. 13 and 14, as well as explained in the specification.

With respect to (2) above, the diodes 852 and 854 and 860 and 862 act as current sources by providing current paths in two different directions. As discussed above, due to the placement of resistor 856 and 858 one of the diode pairs 852 and 854 or 860 and 862 will begin conduction before the other, depending on the polarity of the ESD event. This conduction will convert the voltage of the ESD event into a current that is supplied to terminals A or K, depending on the polarity. As such both diode pairs 852 and 854 or 860 and 862 act as current sources by selectively allowing current to flow along 880 or 890.

With respect to (3) above, Applicants respectfully submit that none of the claims recite that "the base of the bipolar transistor (130 or 150, Fig. 3) can be directly connected to both of the current source (770 or 772) and the resistor (756 or 758)." Claim 8 recites, *inter alia*, "a first current source connected to terminal A and a first end of a first resistor whose second end is connected to terminal K, and a second current source connected to terminal K and a first end of a second resistor whose second end is connected to terminal A." Therefore, the only claimed connection between the first current source, first resistor, second current source, and second resistor is to terminals A and K. With respect to Figs. 13 and 14, the connection shown between the current sources or diode pairs and the base of inherent transistors (130 or 150) is through terminals A and K, and more specifically through regions 124 and 122 of ESD protection structure 100. The connections depicted in Figs. 13 and 14 are schematic equivalents of an ESD protection structure not the actual connections themselves.

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For each of the above reasons, the rejection under 35 U.S.C. § 112, first paragraph is respectfully traversed.

V. Claim Rejections Under 35 U.S.C. § 103(a)

a. Claims 1-3 and 5-7

Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (4,947,226) in view of Kim (5,844,280).

Claim 1 has been cancelled and therefore the rejection with respect to Claim 1 is now moot. Claims 2, 3, and 5-7 have been amended to depend from Claim 8 and are therefore allowable for at least the same reasons as described with respect to Claim 8 in Section V. b. below.

b. Claims 8-10

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al., in view of Kim and further in view of Jonassen (3,890,453). Claim 9 has been cancelled and therefore the rejection with respect to Claim 9 is now moot.

Jonassen discloses that "Zener diodes 13 and 14 are coupled directly across gas tube arrester 11 in back-to-back configuration without requiring current limiting protective resistors between each Zener diode and the electrode to which it is coupled." (Col. 3, ll. 56-60). Further, "[b]y interrelating the threshold level of actuation of gas tube arrester 11, with the operative characteristics of Zener diodes 13 and 14, the need for current limiting resistors in the coupling between each Zener diode and its respective electrode is eliminated." (Col. 3, ll. 60-64). During the occurrence of "a line imbalance across lines 12-12' of a value in excess of 5 volts, the back-to-back Zener diode configuration consisting of Zener diodes 13 and 14 is rendered conductive and a conductive path across line pair 12-12' via said Zener diode configuration shunts the flow of current across any electrical apparatus 15 coupled across said line pair." (Col. 4, ll. 19-28). Therefore, Jonassen discloses a pair of back-to-back Zener diodes that serve as a shunt path for current that is operative in *both* directions.

Claim 8, as amended, recites, *inter alia*, "a first current source connected to terminal A and a first end of a first resistor whose second end is connected to terminal K, and a second current source connected to terminal K and a first end of a second resistor whose second end is connected to terminal A." This configuration is not taught or disclosed in Jonassen. Further, since Jonassen discloses a shunt path for current that is operative in *both* directions, it

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cannot suggest two different current paths, one of which is to trigger in one direction faster than the other. Claim 8 is allowable for at least this reason.

In addition, Applicants respectfully submit that one of ordinary skill in the art would lack the motivation to combine the disclosures of Huang et al. with Jonassen. Jonassen utilizes Zener diodes in order to provide switching times of less than 1 microsecond when a high voltage is applied. (Col. 4, l. 61 - Col. 5, l. 11). However, Jonassen then states that "the back-to-back diode configuration consisting of Zener diodes 13 and 14 ... cannot operate under a sustain[able] and continuous overvoltage imbalance condition when said voltage imbalance levels are excessive without destroying itself." (Col. 5, ll. 34-42). In order to solve this problem, a "three electrode gas tube arrester 11 to carry the burden of shunting across said line pair for the major portion of any excessive line imbalance condition" is provided. (Col. 5, ll. 43-46). Applicants submit that if Huang et al. is used as an ESD protection device it will have a turn-on time that is not substantially different than that of Zener diodes 13 and 14. This is because both structures are semiconductor devices and operate according to the same principles. In addition, a transistor structure such as that in Huang et al. can be doped and configured to have a greater robustness than that of a Zener diode pair. Huang et al. provide a structure that has substantially the same turn-on time as the Zener diode pair and a greater robustness. Therefore, Huang et al. solves the same problems that Zener diode pair of Jonassen and one of ordinary skill in the art would lack the motivation to combine any teachings from Jonassen with Huang et a.

Claims 2, 3, 5-7 and 10 depend from Claim 8 and are therefore allowable for at least the same reasons as discussed with respect to Claim 8.

VI. New Claims

New Claims 21-29 are fully supported by the specification, add no new matter, and contain limitations not taught or disclosed in Yoshioka et al. As such, Applicants respectfully submit that Claims 19-24 are allowable.

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Conclusion

For the above reasons, Applicants respectfully request allowance of Claims 2, 3, 5-8, 10 and 21-30. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 453-9200, extension 1338.

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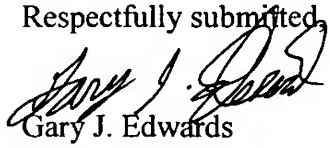
Respectfully submitted,



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In the Specification

This application is a continuation application of U.S. patent application, serial no. 09/100,384, now U.S. Patent No. 6,365,924, entitled "A Dual-Direction Over-Voltage And Over-current IC Protection Device and Its Cell Structure," by Wang et al., assigned to National Semiconductor Corporation [Advanced Micro Devices, Inc.], which is also the Assignee of the present application.

In the Claims

Please amend Claims 2, 3, 5-8 and 10 as follows.

2. (Amended) The ESD protection structure of Claim 8[1], wherein said first conductivity type is an n-type semiconductor and said second conductivity type is a p-type semiconductor.

3. (Amended) The ESD protection structure of Claim 8[1], wherein said first conductivity type is a p-type semiconductor and said second conductivity type is an n-type semiconductor.

5. (Twice Amended) The ESD protection structure of Claim 8,[1] wherein said third semiconductor region includes an n-well region formed in a p-type semiconductor substrate.

6. (Amended) The ESD protection structure of Claim 5, wherein said second and said fourth semiconductor regions each include a p-base region formed in said n-well region.

7. (Amended) The ESD protection structure of Claim 6, wherein said first and said fifth semiconductor regions each include an n^+ region formed in one of said p-base regions.

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8. (Amended) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit comprising: [The ESD structure of Claim 1 further comprising]

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type in contact with said first semiconductor region;

an electrically floating third semiconductor region of said first conductivity type in contact with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type in contact with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region;

a fifth semiconductor region of said first conductivity type in contact with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region; wherein a first terminal, A, of said ESD structure is connected to said first semiconductor region and said second semiconductor region and a second terminal, K, of said ESD structure is connected to said fourth semiconductor region and said fifth semiconductor region;

a first current source connected [across] to terminal A and a first end of a first resistor whose second end is connected to terminal K; and

a second current source connected [across] to terminal K and a first end of a second resistor whose second end is connected to terminal A.

10. (Amended) The ESD protection structure of Claim 8,[9] wherein said first and said second current sources each include a pair of back-to-back Zener diodes.

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